HIBIKI

HIBIKI SDS MANUAL

String Decoding System Fully Discrete DAC

HIBIKI

SDS

SOURCE   Sfreq   Srate   PLL   Locked

SOURCE   MUTE   PHASE   PLL   Extclk
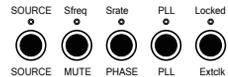
FRONT PANEL
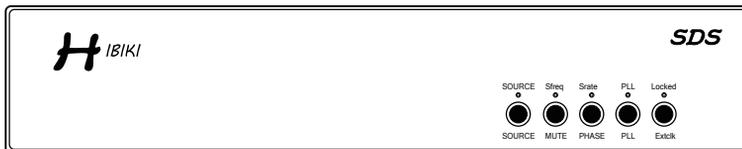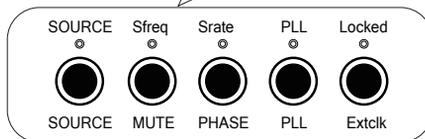
BUTTONS

1.**SOURCE**
Switch in order: AES/EBU(default) -> SPDIF.RCA -> SPDIF.BNC-> TOSLINK-> USB-> HDMI

This button is always lighted.

2.**MUTE**
Normal operation(default) -> Muted
This button is only lighted when muted.

3.**PHASE**
Normal operation(default) -> 180 degree inverted
This button is only lighted when inverted.

4.**PLL**
Switch in order: Bypass(default) -> Wide -> Narrow
This button is always lighted.

5.**ExtClk**
Internal clock in use(default) -> external clock enabled
This button is only lighted when enable external clock source.

LEDS

1.**SOURCE:**

(a)AES/EBU : blue   (b)SPDIF.RCA :green   (c)SPDIF.BNC : cyan   (d)TOSLINK : red
(e)USB : violet   (f)HDMI(I2S) : yellow

2.SFreq:

(a)44.1k PCM : green   (b)44.1k DSD : yellow   (c)48k PCM : blue   (d)48k DSD : violet

3.SRate:

(a)PCM 1x / DSD64x : green   (b)PCM 2x / DSD 128x : red   (c)PCM 4x / DSD 256x : yellow
(d)PCM 8x / DSD 512x : blue   (e)PCM 16x / DSD 1024x : violet

4.PLL:

(a)PCM 1x / DSD64x : green   (b)PCM 2x / DSD 128x : red   (c)PCM 4x / DSD 256x : yellow
(d)PCM 8x / DSD 512x : blue   (e)PCM 16x / DSD 1024x : violet

5.Locked:

(a)Lighted when locked

BACK PANEL
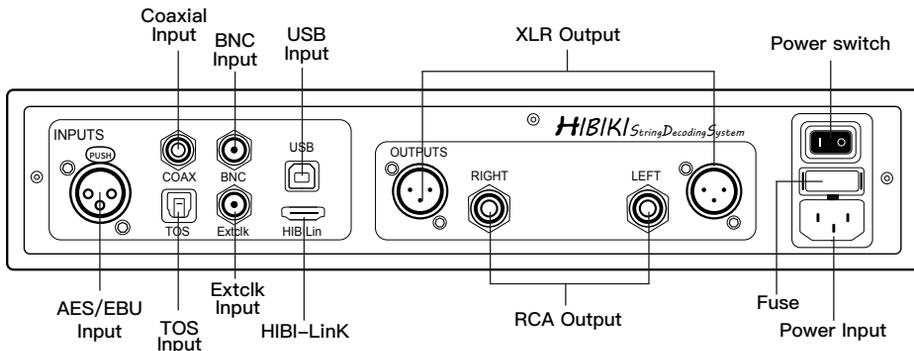
1.AES/EBU:

Support 16~24bit, 44.1kHz~192kHz PCM

2.SPDIF1 RCA:

Support 16~24bit, 44.1kHz~192kHz PCM

3.SPDIF2 BNC:

Support 16~24bit, 44.1kHz~192kHz PCM.
This interface can also be used as an
auxiliary clock port

4.USB:

Support 16~24bit, 44.1kHz~768kHz PCM, 64x~1024x DSD

5.HIBI-Link:

Support 16~24bit, 44.1kHz~768kHz PCM,
64x~1024x DSD, PSAudio protocol I2S

6.ExtClk:

The main clock input port supports 44.1kHz, 48kHz and
its multiplier to 22.5792MHz, 24.576MHz.The minimum
voltage range supports 0.1vpp square wave or 1vpp sine wave.

OUTPUTS

XLR : Maximum output: 14vpp
RCA : Maximum output: 7vpp

SPECIFICATION

330mm

H *IBIKI*

SDS

SOURCE Sfreq Srate PLL Locked

SOURCE MUTE PHASE PLL Extclk

66mm
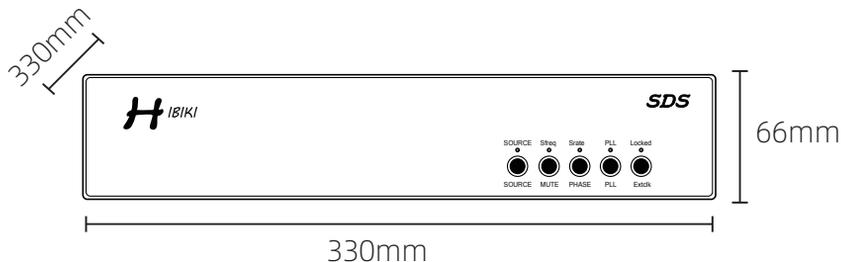
330mm

Technology Highlights

1.Digital Signal Conditioner

2.Ultra-low phase noise re-clocking

3.Digital Filter

4.Delta-Sigma Modulator

5.String Decoding network

6.Discrete Class-A non-negative-feedback
  output stage

Unit dimension
330mm x 330mm x 66mm

Package dimension
400mm x 400mm x 80mm

Package weight
9.5KG

QUICK GUIDE　　　　　　　RECOMMENDED SETUPS

1.SOURCE

We recommend to use RCA coaxial input to get the best sound quality.a.There is no need to worry about the deterioration of sound quality caused by the coaxial phase noise ,because the SDS/BDS internal use of very low phase noise phase locked loop circuit.There is also no need to worry about the extremely strong front end will cause deterioration because the phase-locked loop of this machine, we have carefully studied the market's top CD turntables, USB interfaces,webcast and other audio source equipment, and have selected one that can greatly retain their sound quality and individual PLL configuration . You can rest assured to use all the excellent audio sources and it will not bring deterioration.

We recommend to use the HDMI interface (PS Audio protocol) as the best performance and quality of this machine. At the beginning of design, we configured the HDMI signal as direct pass-through to decoding array . If the HDMI signal quality you provide is excellent, it will send the input signal directly into the decoding array without reservation; If you are not sure about the HDMI quality of the audio source, we will still provide a PLL for your use .

2.CLOCKING
We offer three types of PLL for configuration.
(A)Bypass (PLL light is green) : This configuration does not re-trigger through any PLL. All signals will pass directly through the decoding array. Please use this configuration when you are most confident in the performance of the front-end audio source and want to preserve its audio quality.

(b)Wide (PLL light is red) : This configuration passes through a low phase noise wide bandwidth PLL circuit, all signals are re-triggered through a large-capacity FIFO, and precise controlled timing to send to the decoding array. This configuration can effectively filter the unclean phase noise at the far end, and the performance at the near end is partially preserved. Please use it when you have partial but not complete trust in the front-end audio source. This mode can retain most of the front-end tone and provide cleaner remote information.

(C)Narrow (PLL light is yellow): This configuration uses a very low phase noise and narrow bandwidth PLL circuit. All signals are re-triggered through a large-capacity FIFO, which effectively filters out 90% of the phase noise from most dirty audio sources. The reason for the configuring 90% is that we still want to retain some of the personality of the front end ,even though they may have poor signal quality .

We also offer two options for reference clock sources

(A)Internal clock reference (extclk light is off): This configuration uses the clock source of the front-end audio source as the reference of the PLL, which can preserve the sound characteristics of the front-end.

(B)External clock reference (extclk light is on): This configuration abandons the sound clock as the reference clock source of the PLL and only keeps the clock frequency information.At this point, the clock source of the PLL is an external clock, SDS/BDS will detect the frequency information of the external clock and use this clock as the reference clock of the PLL, it completely ignoring the personality of the front-end sound source, and completely follows the sound characteristics of the external clock.b.In this mode, when the quality of the external clock is much higher than the quality of the internal reference clock of the sound source, the sound quality is improved significantly. This mode is particularly well suited with a broadband PLL (PLL light is red) to retain as much of the superior near-end performance of the external clock as possible while cleaning out the far phase noise degradation caused by wire connectors and logic devices.

TECHNICAL DATA

HIBIKI String Decoding System

AES/EBU	Large scale FIFOs	post signal processing
SPDIF.RCA	DSD only	
SPDIF.BNC	PCM only	encryption engine
TOSLINK	Low noise narrow band fast response analog PLL	Ultra low phase noise VCXOs
USB		clock control
HIBILINK	Low noise wide band fast response analog PLL	Ultra low phase noise LCVCO
extClk		mute control
		phase control
		misc......

ultra low phase noise line reciever

Left Chn & config

Right Chn & config

Low noise fast response power supply: over 50,000uF, 42 LDOs

PowerBase

TECHNICAL DATA